## REMARKS

Applicant respectfully traverses and requests reconsideration.

Applicant thanks the Examiner for notice that claims 16-23 are allowable and that claims 2-6 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully notes that the present Office Action fails to address previously presented claim 24. For at least this reason, Applicant respectfully requests that any subsequent action be non-final.

Claim 1 has been amended to correct a typographical error and to further clarify the claimed subject matter. For instance, the claim now expressly states that "each of the computing devices having a respective one of a plurality of different threshold voltages," as suggested by the Examiner in the previous Office Action.

Claims 1, 7-10, and 14-15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,380,798 to Mizuno et al. ("Mizuno"). Mizuno appears to be directed toward a semiconductor integrated circuit apparatus comprising a circuit 100 including a PMOS transistor and an NMOS transistor where the drain of the PMOS transistor is coupled to the drain of the NMOS transistor. Only the PMOS transistor is coupled to receive a power supply voltage, Vdd, from the power supply voltage control circuit. (Col. 7, ll. 17-35; Fig. 1). Each of the NMOS transistor and the PMOS transistor receive a respective substrate bias voltage as supplied by the substrate bias control circuit 102. (*Id.*).

As to claim 1, the present Office Action states the "plurality of computing devices" is met by circuit 100 of Mizuno's Fig. 1. To the extent circuit 100 and its constituent NMOS transistor and PMOS transistor may be compared to the claimed plurality of computing devices, Applicant

respectfully notes that only the PMOS transistor receives the power supply voltage. However, the claim requires, among other things, that "each of the plurality of computing devices being operative to receive a supply voltage from the dynamic voltage supplier." Accordingly, for at least the reason that Mizuno does not include a plurality of computing devices where each is operative to receive a supply voltage from the dynamic voltage supplier, claim 1 is in condition for allowance.

Claim 6 has been amended to clarify the claimed subject matter.

Claims 7-9 depend upon allowable claim 1 and further contain additional novel and non-obvious subject matter not present in the cited prior art. For at least this reason, claims 8-9 are also believed to be in proper condition for allowance.

Claim 10 has been amended to clarify the claimed subject matter. As to claim 10, Applicant respectfully reasserts the relevant remarks made above with respect to claim 1. For at least the reason that Mizuno does not teach "providing the supply voltage to each of a plurality of computing devices," claim 10 is also believed to be in proper condition for allowance.

Claim 13 has been amended to clarify the claimed subject matter.

Claims 14 and 15 depend upon allowable claim 10 and further contain additional novel and non-obvious subject matter not present in the cited prior art. For at least this reason, claims 14-15 are also believed to be in proper condition for allowance.

Claim 24 has been amended to clarify the claimed subject matter. Applicant respectfully reasserts the relevant remarks made above with respect to claim 1 and for at least the same reasons articulate, claim 24 is believed to be allowable over the cited prior art.

Claim 25 has been added. Claim 25 recites that the plurality of computing devices comprises "a first computing device and a second computing device, wherein each ... comprises

at least two transistor devices operatively coupled in a push-pull configuration; and wherein an output of the first computing device is operatively coupled to an input of the second computing device." Because at least the cited portion of Mizuno appears to be directed toward a single circuit having an NMOS transistor and a PMOS transistor and does not appears to be directed toward a first and a second computing device, each comprising at least two transistor devices operatively coupled in a push-pull configuration where an output of the first computing device is coupled to the input of the second computing device, Applicant respectfully believes claim 25 is also in proper condition for allowance.

Applicant respectfully submits that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 7/25/06

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005